Abstract of the Disclosure

The primary objective of the present invention is to provide a data output buffer capable of preventing the phenomenon of a wide data valid window caused from early outputting of the first output data during data output operations. For this purpose, the present invention provides a data output buffer circuit in a semiconductor memory device which includes: a driving part for receiving pull-up and pull-down control signals and driving a data output terminal with a voltage level corresponding to data read from a memory cell; and a controlling part for supplying the driving part with control signals to delay the first output of the read data for a designated delay time, and to cause the output of the driving part to retain high impedance state during the designated delay time.